REMARKS

Claim Rejections – 35 U.S.C. §102

Claims 1 and 2 stand rejected under 35 U.S.C. §102(b) as being anticipated by London (US 6,114,731).

Directing Examiner's attention to MPEP 2131, the threshold issue under Section 102 is whether the Examiner has established a *prima facie* case for anticipation. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim.

Claim 1 recites a transistor formed on a semiconductor substrate of a first conductivity type and comprising "a well formed in said substrate and doped with said first conductivity type to an impurity level higher than that of said substrate; a drain region doped to a second conductivity type opposite to said first conductivity type disposed in said well; a pair of opposed source regions doped to said second conductivity type disposed in said well and separated from opposing outer edges of said drain region by channel regions ... wherein the region of said well doped to an impurity level higher than that of said substrate overlaps said drain region, the overlap being about equal to the channel length of said transistor."

Although Examiner asserts that the drain 212b of London overlaps regions 206 and 306 by an amount about equal to the channel length, Applicant cannot find any discussion in London of the size of the overlap or the size of the channel region. Applicant respectfully submits that London cannot teach the overlap being about equal to the channel length of the transistor if it does not even disclose the size of either one.

Applicant respectfully submits that London fails to disclose each and every element in as complete detail as in Claim 1. Therefore, Applicant respectfully submits

that Claim 1 is currently in condition for allowance. Reconsideration and withdrawal of this rejection is respectfully requested.

The same arguments made above with respect to the patentability of Claim 1 are applicable to the patentability of Claim 2 as well. Therefore, Applicant respectfully submits that Claim 2 is currently in condition for allowance.

Claim Rejections – 35 U.S.C. §103

Claims 3 and 4 stand rejected under 35 U.S.C. §103(a) as being unpatentable over London in view of Rhee (US 6,395,941).

For a §103 obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. MPEP 2143.

Claim 3 recites a transistor disposed on a p-type substrate comprising "a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate; an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate-doped portion of said p-well, said periphery surrounded by a lightly doped N region; a pair of N+ source

regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together ... wherein the portion of said p-well doped to a higher concentration than said substrate overlaps said drain region, the overlap being about equal to the channel length of said transistor."

As discussed above, London does not disclose the overlap of drain 212b with regions 206 and 306 being about equal to the channel length of the transistor, as recited in Claim 3. Furthermore, Applicant cannot find, nor has Examiner cited, any mention of this limitation in Rhee. Since neither London nor Rhee teaches this limitation individually, they cannot teach it in combination.

Therefore, Applicant respectfully submits that Examiner has failed to establish that all elements of the present invention are disclosed in the prior art. Applicant respectfully submits that Claim 3 is currently in condition for allowance. Reconsideration and withdrawal of the rejection is respectfully requested.

Since Claim 4 depends from Claim 3, Applicant respectfully submits that Claim 4 is also patentable as it contains the same limitations as its parent claim. Reconsideration and withdrawal of this rejection is respectfully requested.

If the Examiner has any questions regarding this application, the Examiner may telephone the undersigned at 775-586-9500.

Respectfully submitted,
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